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Automotive Memory Chip and Storage Industry Report, 2024

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The global automotive memory chip market was worth USD4.76 billion in 2023, and it is expected to reach USD10.25 billion in 2028 boosted by high-level autonomous driving.

The automotive storage market is a high-growth semiconductor segment.

Automotive memory chips accounted for about 8-9% of the value of automotive semiconductors in 2023, and the proportion is expected to rise to 10-11% in 2028, mainly because the faster innovation in automotive memory chips promotes the rapid adoption of advanced memory chips into cars. Main driving forces are:

* DRAM: DRAM is the memory chip with the largest market size. In the field of consumer electronics (mobile phones, PCs, tablet PCs, etc.), DDR5 (LPDDR5) has become mainstream and will gradually replace the conventional DDR4 (LPDDR4) in the next 2-3 years. In the automotive field, the conventional DDR is evolving to DDR4, LPDDR3 and LPDDR4, and then to advanced storage products such as LPDDR5 and GDDR6.

* HBM: as the enhanced version of DRAM, HBM provides higher bandwidth and capacity by stacking multiple DRAM chips. Because of high price, it is unlikely to appear in vehicles for a long time, but the cloud server used for training the Transformer AI foundation model must be equipped with multiple HBMs which account for about 9% of the AI server cost, with the ASP (average selling price) per unit as high as USD18,000.

NAND Flash: In the automotive computing system, important data and trained weight models are stored in the hard disk (i.e., eMMC or UFS). NAND generally stores continuous data in ADAS, IVI systems, center consoles, etc. In the trend towards five-domain fusion, a single vehicle will need 2TB+ NAND in the next 3-5 years, and automotive PCIe SSD for central computing will become an important growth engine.

* SRAM: SRAM is much faster than NAND and DRAM but more expensive. Independent SRAM has almost disappeared, and it is mainly integrated directly into CPU, GPU and various SoCs in the form of an IP kernel. High-performance automotive SoCs generally integrate high-capacity on-chip SRAM.

* MRAM: Wafer giants such as Samsung and TSMC are developing MRAM for the next-generation automotive applications. NXP plans to introduce MRAM to its next-generation S32 zonal ECUs and MCUs. The industry believes that MRAM is expected to replace SRAM as cache memory.

* EEPROM: a smart car requires up to 30-40 EEPROM chips, while an ordinary fuel-powered vehicle only needs about 15 EEPROM chips. EEPROM is extending to BMS, intelligent cockpits, gateways, "electric drive, battery, electric control" systems and other applications.

* FRAM: FRAM outperforms conventional Flash and EEPROM in reading and writing durability, writing speed and power consumption, and has been applied to airbag data storage, event data recorder (EDR), new energy vehicle CAN-BOX, new energy vehicle communication terminal (T-BOX) and other fields.

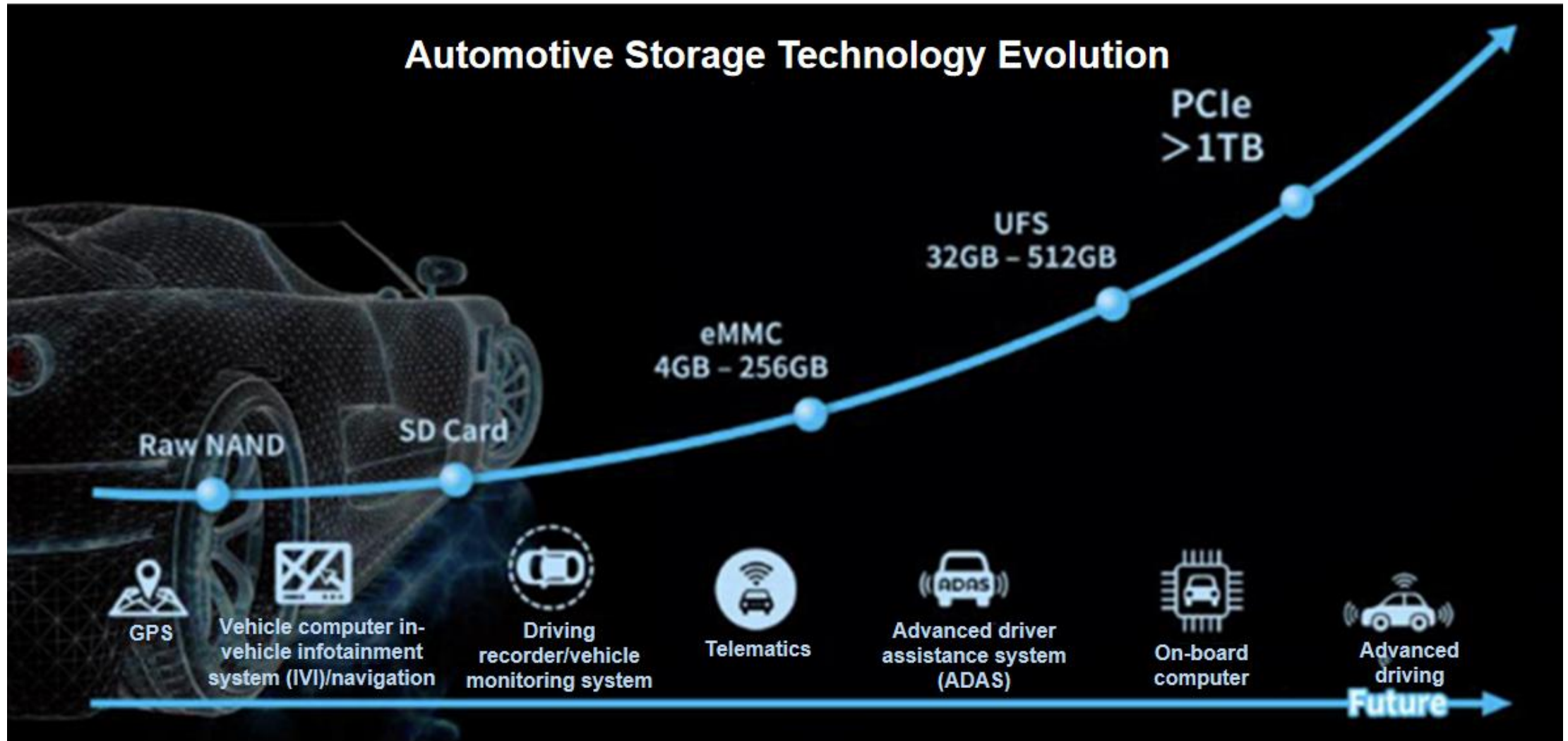
Evolution of automotive NAND Flash memory: UFS 4.0, PCIe SSD for central computing, CXL memory expansion technology

As with a computer system, a current automotive computing system also has a hard disk where important data and trained weight models are stored.

eMMC5.1 and UFS3.1 have become the mainstream standards for automotive NAND Flash memory. In February 2024, KIOXIA announced sampling of the industry's first Universal Flash Storage (UFS) Ver. 4.0 embedded flash memory devices designed for automotive applications in line with AEC-Q100 Grade2 requirements. UFS 4.0 supports theoretical interface speeds of up to 23.2Gbps per lane or 46.4Gbps per device. It is conceivable that by 2025, UFS 4.0 will become one of automotive storage standards, and will be applicable to different automotive EEAs.

In the future, the automotive NVMe SSD based on PCIe interfaces will offer data throughput of more than 10GB/s, and the massive storage capacity will provide strong support for the next-generation intelligent automotive systems. Automotive SSD refers to the solid-state drive with PCIe as the physical layer and NVMe as the communication protocol.

NVMe supports ultra-long queues so as to greatly ease the storage bottleneck problem during parallel computing. In the era of central computing, storage should be integrated into the central computer, and PCIe is the best choice. SSD is connected to the central computing unit SoC via a PCIe switch.

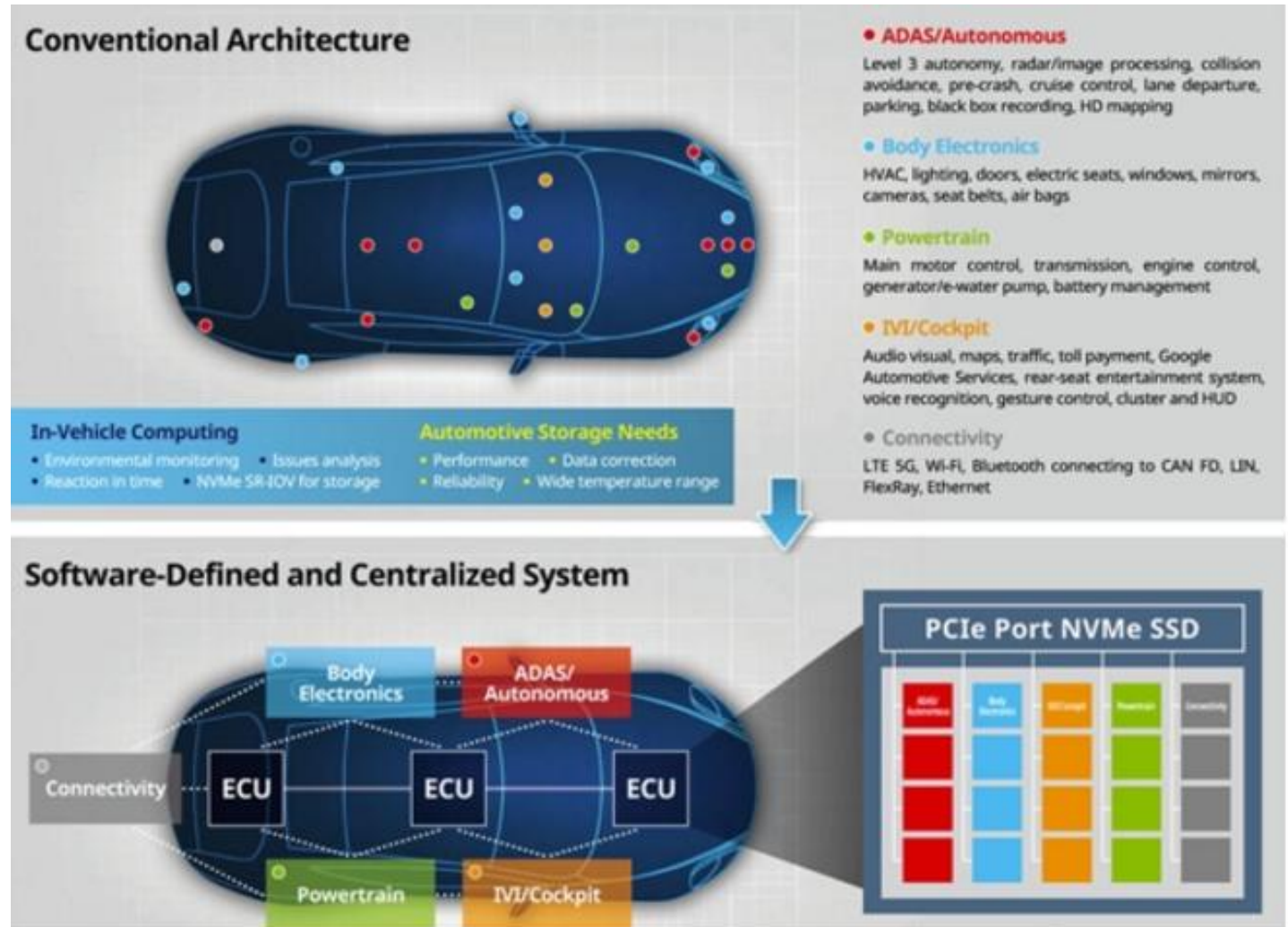


Source: Silicon Motion

JEDEC approved the JESD312 standard

JEDEC, a standard setter in the storage industry, approved the JESD312 standard in November 2022, and officially released it on December 14. JESD312 defines the specifications of interface parameters, signaling protocols, environmental requirements, packaging, and other features for a solid state drive (SSD) targeted primarily at automotive applications. Automotive SSD is directly mounted on PCB in the form of BGA, with the size not larger than 28x28 mm. It uses four PCIe 4.0 interfaces to provide a peak transmission rate of up to 8 Gb/s.

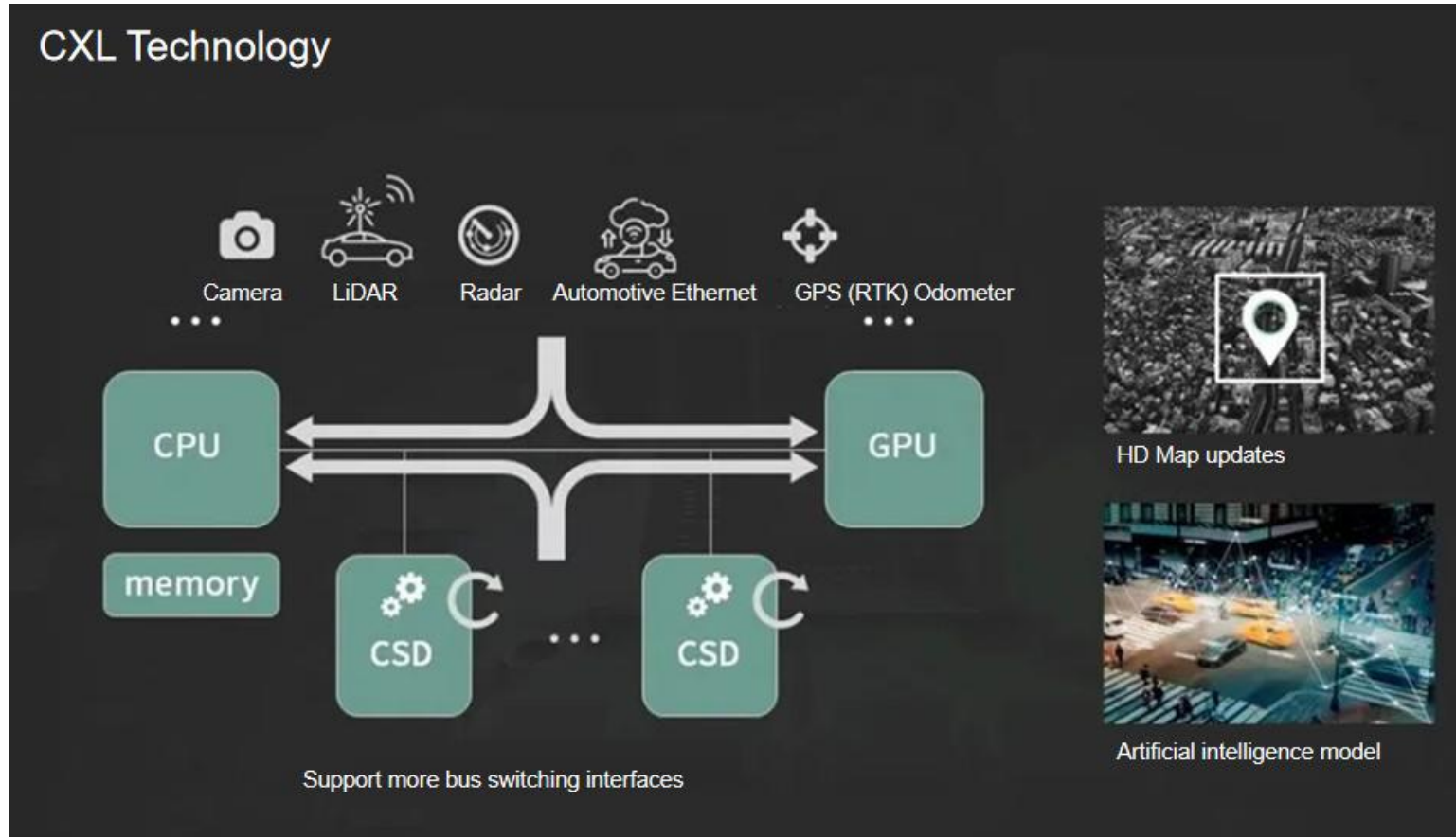
JESD312 takes into a full account the changes of automotive electronic architectures, targets software-defined vehicles and central computing architecture, and allows the storage array to be partitioned.



Source: JEDEC

CXL (Compute Express Link)

CXL (Compute Express Link), a storage technology based on PCIe, will be one of the important development directions of automotive storage in the future. CXL is a new open interconnect standard, and its essence is to change the original hard disk access model into the existing memory access model and exchange data in the form of memory access. CXL enables high-speed and efficient interconnect between CPU and GPU, FPGA or other accelerators, thus meeting the requirements of high-performance heterogeneous computing.



Source: YEESTOR

Evolution of automotive DRAM: In the era of Transformer model, GDDR6 and HBM develop rapidly, and storage cost shoots up.

The key to AI operation lies in storage instead of AI processor. 90% of the power consumption and delay of AI operation come from storage or data transfer. In 90% working conditions, the AI processor is waiting for the storage system to transfer data, and the time required by the computing system is almost negligible, so the performance of the storage system actually determines the real computing power. Wherein, the storage bandwidth can basically be equated to the performance of the storage system and the real computing power.

In the Transformer era, there are at least more than 1 billion model parameters, a model is at least 1GB, and the storage bandwidth determines whether Transformer can be run. In addition, storage dominates power consumption. According to Intel's research, when the semiconductor process reaches 7nm, an AI chip (accelerator) takes as high as 35pJ/bit to transfer data, making up 63.7% of the total power consumption.

Intelligent vehicles pose ever higher requirements for image floating-point operation. To run Transformer smoothly, the weight model should be read up to 200 times per second, so the storage bandwidth should be at least 400GB/s, 600 GB/s better. On this basis, Samsung and Micron plan to launch their own automotive GDDR6 solutions.

In Tesla HW3.0, the storage bandwidth of the first-generation FSD is only 34GB/s, which is difficult to support the next-generation foundation models. Tesla's latest self-driving brain HW4.0 therefore uses GDDR6 at all costs, 16 pieces (2GB per piece) used, with 8 each on the front and back side, plus the 4 GDDR6 chips (also 2GB) in the cockpit controller, totaling 20 pieces (40GB), and the cost is more than USD160. HW3.0 uses 8 LPDDR4 chips, and a total of 8 LPDDR4 RAMs, each with capacity of 1GB, totaling 8GB, and the cost is about USD28.

Tesla HW4.0



Source: ResearchInChina

Memory Bandwidth of Common Automotive Autonomous Driving SoCs

In Tesla HW4.0, GDDR6 is non-automotive-grade D9PZR provided by Micron, and the GDDR6 physical layer of is from Cadence. Rambus also provides the GDDR6 physical layer and earns approximately USD140 million in annual revenue from its storage physical layer IPs. In September 2023, Cadence acquired the SerDes and memory interface PHY IP business from Rambus Inc.

Currently, among Tesla's automotive memory chips, the 2nd-generation FSD has the highest bandwidth ranging from 448Gb/s to 1008GB/s. SK Hynix's HBM2E (H5WG6HMN6QX038R) supports minimum bandwidth of 460GB/s, with the density of 16GB. The dual-channel design allows for 920GB/s, even up to 1840GB/s, but it is still far less cost-effective than GDDR6.

GDDR6 is expected to prevail, and HBM may follow. Tesla HW 5.0 or the third-generation FSD chip may use HBM, but this is a distant future.

Memory Bandwidth of Common Automotive Autonomous Driving SoCs

Vendor	Model	Maximum memory supported	Memory width	Memory bandwidth
Nvidia	Orin	LPDDR5x	256bit	204.8GB/s
Nvidia	Xavier	LPDDR4X	256bit	137GB/s
Qualcomm	SA8155P	LPDDR4X	128bit	68GB/s
Qualcomm	SA8295P	LPDDR4X	256bit	137GB/s
Qualcomm	SA8255P	LPDDR5		
SiEngine Technology	Longying No.1	LPDDR5		51.2GB/s
Huawei	Ascend 310	LPDDR4X	128bit	59.8GB/s
Huawei	Ascend 610	LPDDR4X	256bit (estimated)	137GB/s (estimated)
Tesla	First-generation FSD	LPDDR4	128bit	34GB/s
Tesla	Second-generation FSD	GDDR6	256bit (estimated)	448GB/s (estimated)
Renesas	V4H	LPDDR5	64bit	51.2GB/s
Mobileye	EyeQ5	LPDDR4	32bit	8.5GB/s (estimated)
Mobileye	EyeQ6L	LPDDR4X	64bit (estimated)	17GB/s (estimated)
Mobileye	EyeQ6H	LPDDR5	128bit (estimated)	102.4GB/s (estimated)
Mobileye	EyeQ6 ULTRA	LPDDR5X	128bit (estimated)	136.2GB/s (estimated)
Nvidia	RTX4090	GDD6X	384bit	1008GB/s
Nvidia	RTX3050	GDDR6	128bit	224GB/s

Source: ResearchInChina

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